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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,562	10/17/2003	Yung-Ta Chan	CHAN3220/EM	8978

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EXAMINER	
RICHMOND, LEAH L	
ART UNIT	**PAPER NUMBER**
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/686,562	CHAN ET AL.	
	Examiner	Art Unit	
	Leah L. Richmond	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Brant et al. (U.S. Patent # 7003638)** in view of **Athanas et al. (U.S. Patent Application Publication # 20020184394)** and further in view of **Jorgensen et al. ("MAC layer proposal with IP QoS allowances for BWA").**

Consider **claim 1**, Brant et al. clearly show and disclose a burst transfer mechanism of packets over a USB bus designed in an ASIC installed in a USB compliant device that enables the device to transmit the USB packets out within a burst cycle (Col. 3, lines 52 - 61: "In Fig. 2, an embedded controller 12 is coupled to a memory bus 20 and a PCI bus 30. Embedded controller 12 includes a processor 14, a memory system controller 16, and an I/O system controller 18. Memory bus 20 is coupled to two memory modules 22A and 22B and a peripheral device 32A. PCI bus 30 is coupled to a PCI device 36. PCI bus 36 is illustrated as an exemplary peripheral or I/O bus. Other peripheral bus technologies such as ISA (Industry Standard Architecture) and USB (Universal Serial Bus) may be used in other embodiments." and Col. 5, lines 38 - 42: "Interface 200 within peripheral device 32A may include system configuration and control registers that store parameters indicating certain memory module parameters such as default burst length, control signal pulse widths, timing mode, etc." and Col. 5, line 65 – Col. 6, line 7: "For example, interface 200 may include registers that support optional interrupt and/or polled status operation of transfers to peripheral device 32A. Such registers may be used to provide packet and/or frame flow control between a peripheral device such as an Ethernet MAC and embedded controller 12. The interface 200 included in peripheral device 32A may be configured to

participate in burst transfers on memory bus 20 according to a particular memory standard supported by the system memory controller 16."). Brant et al. do not disclose transferring a super-size network packet into a plurality of USB packets having maximum packet size defined for the USB endpoint while receiving a Bulk In/Out request packet. However, Athanas et al. clearly show and disclose translating an ethernet MAC frame into USB packets (paragraph [0029]: "The data storage system 50 includes an Ethernet interface 60, a controller system 80, a memory 90, and a common housing 100. The Ethernet interface 60 is configured to receive and to send Ethernet packets according to a first protocol, which is in a format useable by a client system. The memory 90 stores and retrieves data according to a second protocol. The controller system 80 is coupled between the Ethernet interface 60 and the memory 90 to translate between the first protocol and the second protocol. The Ethernet interface, memory, and controller system are preferably disposed within a common housing. The memory 90 is capable of forming a response to a request from the client system, including: storing information, retrieving information, and providing status information. The second protocol can support communication with standard memory devices including without limitation: ATA, SCSI, USB, USB-2, Firewire, and the like."). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate translating an Ethernet MAC packet into USB packets, as taught by Athanas et al., in the burst transfer mechanism of network packets having MAC frames over USB bus as in Brant et al. for the purpose of translating network packets having MAC frames into USB format for transmission over a

USB bus. Brant et al. in view of Athanas et al. do not disclose assembling a plurality of Ethernet network packets having MAC frames together as a super-size network packet. However, Jorgensen et al. clearly show and disclose assembling a plurality of Ethernet network packets having MAC frames together as a super-size network packet (Section 2. MAC Multiplexing for downstream transmission: "We propose the provision for multiplexing IP packets within one MAC frame. DOCSIS 1.1 only allows multiplexing of individual MAC frames in the MAC TC layer but not in the MAC layer for downstream traffic, although concatenation of MAC frames is presently allowed for upstream traffic. This proposal includes a second concatenated MAC header format (see Figure 3) to further improve bandwidth utilization. Here each data PDU is an IP packet without a MAC header. The variable length multiplexed MAC frame is most suitable for the placement of several short IP packets into one MAC frame. The saving is 6 bytes (MAC frame header) per IP packet."). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate assembling a plurality of Ethernet network packets into a super-size packet, as taught by Jorgensen et al., in the burst transfer mechanism as in Brant et al. in view of Athanas et al. for the purpose of using bandwidth more efficiently.

Claims 2 and **4** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Brant et al. (U.S. Patent # 7003638)** in view of **Athanas et al. (U.S. Patent Application Publication # 20020184394)** and further in view of **Jorgensen et al.**

("MAC layer proposal with IP QoS allowances for BWA") and further in view of **Senior et al. (U.S. Patent # 6898654).**

Consider **claim 2**, and as applied to claim 1, Senior et al. clearly show and disclose a networking device receiving an I/O request packet and transmitting this packet to a USB driver installed therein (Col. 7, lines 3 -15: "USB specifications require a USB driver to handle I/O Request Packet (IRP). Use of an IRP is a well known, but not the only strategy, for an operating system to facilitate drivers providing services to applications and other software executing on a computer system. In an embodiment described in the instant application, the standardized format offered by IRP and I/O control functions (IOCTL) can be advantageously used to allow addressing drivers, including the USB driver and associated devices drivers. Thus, extending the capabilities of the USB may be efficiently managed by suitably designed interfaces and IRPs to request that USB, and devices connected to the USB, behave in a desired manner." and Col. 7, line 66 – Col. 8, line 1: "The device drivers, including those for the hubs, are loaded and process requests from the system for services. These requests are usually in the form of (IRPs)." and Col. 8, lines 8 - 10: "An IRP is constructed when needed. A given IRP may be passed from one driver to another as needed to allow all of the requested functions to be completed."). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate sending an I/O request packet to the USB driver, as taught by Senior et al., in the burst transfer mechanism of network packets having MAC frames over USB bus as in Brant et al. in view of Athanas et al. and further in view of Jorgensen et al. for the purpose of

requesting a service from the USB driver. Senior et al. do not disclose assembling a plurality of network packets having MAC frames together into a super-size packet. However, Jorgensen et al. clearly show and disclose assembling a plurality of Ethernet network packets having MAC frames together as a super-size network packet (Section 2. MAC Multiplexing for downstream transmission: "We propose the provision for multiplexing IP packets within one MAC frame. DOCSIS 1.1 only allows multiplexing of individual MAC frames in the MAC TC layer but not in the MAC layer for downstream traffic, although concatenation of MAC frames is presently allowed for upstream traffic. This proposal includes a second concatenated MAC header format (see Figure 3) to further improve bandwidth utilization. Here each data PDU is an IP packet without a MAC header. The variable length multiplexed MAC frame is most suitable for the placement of several short IP packets into one MAC frame. The saving is 6 bytes (MAC frame header) per IP packet.").

Consider **claim 4**, and as applied to claim 2, Brant et al. in view of Athanas et al. and further in view of Jorgensen et al. and further in view of Senior et al. clearly show and disclose the USB driver granting the request of the I/O packet after receiving the I/O request packet (Senior et al., Col. 7, line 66 – Col. 8, line 1: "The device drivers, including those for the hubs, are loaded and process requests from the system for services. These requests are usually in the form of (IRPs)." and Col. 8, lines 8 - 10: "An IRP is constructed when needed. A given IRP may be passed from one driver to another as needed to allow all of the requested functions to be completed."), the mechanism proceeding with the capsulation process with respect to the super-size

network packet, transferring the super-size network packet into a plurality of USB packets (Athanas et al., paragraph [0029]: "The data storage system 50 includes an Ethernet interface 60, a controller system 80, a memory 90, and a common housing 100. The Ethernet interface 60 is configured to receive and to send Ethernet packets according to a first protocol, which is in a format useable by a client system. The memory 90 stores and retrieves data according to a second protocol. The controller system 80 is coupled between the Ethernet interface 60 and the memory 90 to translate between the first protocol and the second protocol. The Ethernet interface, memory, and controller system are preferably disposed within a common housing. The memory 90 is capable of forming a response to a request from the client system, including: storing information, retrieving information, and providing status information. The second protocol can support communication with standard memory devices including without limitation: ATA, SCSI, USB, USB-2, Firewire, and the like."), and then transmitting the USB packets out within a burst cycle (Brant et al., Col. 5, line 65 – Col. 6, line 7: "For example, interface 200 may include registers that support optional interrupt and/or polled status operation of transfers to peripheral device 32A. Such registers may be used to provide packet and/or frame flow control between a peripheral device such as an Ethernet MAC and embedded controller 12. The interface 200 included in peripheral device 32A may be configured to participate in burst transfers on memory bus 20 according to a particular memory standard supported by the system memory controller 16.").

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Brant et al. (U.S. Patent # 7003638)** in view of **Athanas et al. (U.S. Patent Application Publication # 20020184394)** and further in view of **Jorgensen et al. ("MAC layer proposal with IP QoS allowances for BWA")** and further in view of **Senior et al. (U.S. Patent # 6898654)** and further in view of **Kalliokulju et al. (U.S. Patent Application Publication # 2003/0063569).**

Consider **claim 3**, and as applied to claim 2, Kalliokulju et al. clearly show and disclose delineating the boundaries between packets in a traffic stream by using extra bytes (paragraph [0054]: "A marker field 212 (1 bit) allows significant points to be marked in the traffic stream. For example, frame boundaries can be marked by the marker field 212."). Kalliokulju et al. also disclose using bytes to indicate length (paragraph [0054]: "The third and fourth octets of this header extension indicate its length."). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the disclosure in Kalliokulju et al. and use bytes indicating the packet length as boundary markers to indicate the ending position of each MAC frame network packet in the burst transfer mechanism of network packets having MAC frames over USB bus as in Brant et al. in view of Athanas et al. and further in view of Jorgensen et al. and further in view of Senior et al. for the purpose of marking significant points in the super-size packet.

Claims 5 and **6** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Brant et al. (U.S. Patent # 7003638)** in view of **Athanas et al. (U.S. Patent**

Application Publication # 20020184394) and further in view of **Jorgensen et al. ("MAC layer proposal with IP QoS allowances for BWA")** and further in view of **Senior et al. (U.S. Patent # 6898654)** and further in view of **Smith et al. (U.S. Patent # 6222823)**.

Consider **claim 5**, and as applied to claim 4, Smith et al. clearly show and disclose predefining a burst credit in terms of number of bytes to determine the maximum size of network packet that can be sent during a burst cycle (Col. 12, lines 23 - 25: "The cell stream fed to output 32 is shaped by the shaper so that bursts which are not greater than the burst tolerance t pass without being delayed by the shaper 62." and lines 35 - 37: "Cells will be forced to wait by the shaper function if bursts arrive which are longer than the burst tolerance credit value." and lines 43 – 45: "receive a cell.waiting [VPI/VCI] signal from buffer IF burst credit ok THEN cell.can.go: = TRUE"). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate predefining a burst credit in terms of bytes, as taught by Smith et al., in the burst transfer mechanism of network packets having MAC frames over USB bus as in Brant et al. in view of Athanas et al. and further in view of Jorgensen et al. and further in view of Senior et al. for the purpose of not allowing the size of the packet to exceed the available bandwidth in the burst cycle.

Consider **claim 6**, and as applied to claim 4, Smith et al. clearly show and disclose predefining a burst credit in terms of number of bytes according to the number of packets currently queued in a buffer to determine the maximum size of network packet that can be sent during a burst cycle (Col. 6, lines 52 - 54: "The pre-

transmission buffering of the DBC [Dynamic Bandwidth Controller] is used to allow a cooperating end-system sufficient time to adjust its output to the latest CR feedback advice." And Col. 8, lines 48 - 51: "For the time being, it is sufficient simply to say that the buffer module is capable of signaling to the controller 38 when any buffer queue has reached a predetermined buffer fill threshold." Col. 12, lines 23 - 25: "The cell stream fed to output 32 is shaped by the shaper so that bursts which are not greater than the burst tolerance t pass without being delayed by the shaper 62." and lines 35 - 37: "Cells will be forced to wait by the shaper function if bursts arrive which are longer than the burst tolerance credit value." and lines 43 – 45: "receive a cell.waiting [VPI/VCI] signal from buffer IF burst credit ok THEN cell.can.go: = TRUE"). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate predefining a burst credit in terms of number of bytes according to the number of packets currently queued in a buffer to determine the maximum size of network packet that can be sent during a burst cycle, as taught by Smith et al., in the burst transfer mechanism of network packets having MAC frames over USB bus as in Brant et al. in view of Athanas et al. and further in view of Jorgensen et al. and further in view of Senior et al. for the purpose of determining the size of the burst credit according to the number of packets waiting to be transmitted.

Conclusion

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

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P.O. Box 1450
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Hand-delivered responses should be brought to

Customer Service Window
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401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Leah Richmond whose telephone number is (571) 270-1774. The Examiner can normally be reached on Monday-Thursday from 9:00am to 6:00pm Eastern Standard Time.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rafael Pérez-Gutiérrez can be reached at (571) 272-7915. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 703-305-3028.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Leah Richmond
L.L.R./llr

April 25, 2007

RAFAEL PEREZ-GUTIERREZ
SUPERVISORY PATENT EXAMINER
4/25/07